IN THE CLAIMS:

Please amend claims 1, 4, 7, 8, 11, 14, 15, 18-20, and 23, and add new claims 35-38 as follows:

1. (Currently Amended) An integrated circuit having a plurality of active components including junctions formed in a monocrystalline substrate doped locally, and at least one passive component situated above the active components, said integrated circuit comprising:

a first insulating layer separating the active components and a base of the passive component; and

a metal terminal for electrically connecting the passive component with at least one of the active components, the metal terminal being formed in the thickness of the first insulating layer, ~~and~~ having a lower surface that contacts a junction of the one active component such that the lower surface of the metal terminal extends over a boundary of the junction of the one active component, and having an upper surface that contacts the base of the passive component,

wherein the metal terminal consists of a single layer of metal extending from the junction of the one active component to the base of the passive component.

2. (Original) The integrated circuit according to claim 1, wherein the passive component is a capacitor.

3. (Original) The integrated circuit according to claim 1, wherein the passive component is an inductor.

4. (Currently Amended) The integrated circuit according to claim 1,

wherein the thickness of the first insulating layer is greater than 0.3 micrometers,

the top surface of the first insulating layer is plane, and

the metal terminal is made ~~principally~~ of tungsten.

5. (Original) The integrated circuit according to claim 1, further comprising a second insulating layer above the first insulating layer, the passive component being set into a cavity formed throughout the thickness of the second insulating layer.

6. (Original) The integrated circuit according to claim 5, wherein the thickness of the second insulating layer is greater than 2 micrometers.

7. (Currently Amended) An integrated circuit including a plurality of transistors, a plurality of passive components, and a level of local metal connections formed within a first insulating layer that is deposited on top of the transistors of the integrated circuit, said integrated circuit comprising:

a first metal terminal passing completely through the thickness of the first insulating layer, the first metal terminal constituting a first stage of contact between ~~an~~ one active area of the integrated circuit and a first level of interconnection, and having an upper surface that contacts a second stage of contact between the one active area of the integrated circuit and the first level of interconnection;

a second metal terminal passing completely through the thickness of the first insulating layer, the second metal terminal vertically connecting ~~an~~ one active area of the integrated circuit to a passive component that directly contacts the upper surface of the first insulating layer; and

a third metal terminal passing completely through the thickness of the first insulating layer, the third metal terminal horizontally connecting two separate active areas of the integrated circuit,

wherein the first metal terminal consists of a single layer of metal extending from the one active area of the integrated circuit to the second stage of contact, and

the third metal terminal consists of a single layer of metal.

8. (Currently Amended) The integrated circuit according to claim 7, wherein the second metal terminal has a lower surface that contacts a junction of one of the transistors of the integrated circuit such that the lower surface of the second metal terminal extends over a boundary of the junction of the one transistor.

9. (Original) The integrated circuit according to claim 7, wherein the passive components include capacitors.

10. (Original) The integrated circuit according to claim 7, wherein the passive components include inductors.

11. (Currently Amended) The integrated circuit according to claim 7,
wherein the thickness of the first insulating layer is greater than 0.3 micrometers,
the top surface of the first insulating layer is plane, and
the first, second, and third metal terminals are made ~~principally~~ of tungsten.

12. (Original) The integrated circuit according to claim 7, further comprising a second insulating layer above the first insulating layer, the passive component resting on the first insulating layer being set into a cavity formed throughout the thickness of the second insulating layer.

13. (Original) The integrated circuit according to claim 12, wherein the thickness of the second insulating layer is greater than 2 micrometers.

14. (Currently Amended) An integrated circuit comprising:

an onboard memory plane of DRAM cells in a matrix, each of the cells including a control transistor and a storage capacitor;

a plurality of MOS transistors;

a first level of interconnection above the storage capacitors;

a first insulating layer separating the MOS transistors and the base of the storage capacitors; and

a level of local connections including three metal terminals each opening onto each side of the first insulating layer,

wherein the first metal terminal forms a first stage of contact between one active area of the integrated circuit and the first level of interconnection, has an upper surface that contacts a second stage of contact between the one active area of the integrated circuit and the first level of interconnection, and consists of a single layer of metal extending from the one active area of the integrated circuit to the second stage of contact,

the second metal terminal vertically connects one active area of the integrated circuit with one plate of one of the storage capacitors, the one plate of the one storage capacitor directly contacting the upper surface of the first insulating layer, and

the third metal terminal horizontally connects two separate active areas of the integrated circuit, and consists of a single layer of metal.

15. (Currently Amended) The integrated circuit according to claim 14, wherein the second metal terminal has a lower surface that contacts a junction of the one active area such that the lower surface of the second metal terminal extends over a boundary of the junction of the one active area.

16. (Original) The integrated circuit according to claim 14, further comprising:

a second insulating layer above the first insulating layer; and

a cavity passing through the entire thickness of the second insulating layer and opening onto the top surface of the second metal terminal,

wherein the one plate of the one storage capacitor carpets the bottom and the inside flanks of the cavity.

17. (Original) The integrated circuit according to claim 16, further comprising:

a third insulating layer above the second insulating layer; and

a contact opening passing through the second insulating layer and the third insulating layer and opening onto the top surface of the first metal terminal.

18. (Currently Amended) The integrated circuit according to claim 14, wherein the first, second, and third metal terminals are made ~~principally~~ of tungsten.

19. (Currently Amended) An information processing system including at least one integrated circuit, the integrated circuit comprising:

an onboard memory plane of DRAM cells in a matrix, each of the cells including a control transistor and a storage capacitor;

a plurality of MOS transistors;

a first level of interconnection above the storage capacitors;

a first insulating layer separating the MOS transistors and the base of the storage capacitors; and

a level of local connections including three metal terminals each opening onto each side of the first insulating layer,

wherein the first metal terminal forms a first stage of contact between one active area of the integrated circuit and the first level of interconnection, has an upper surface that contacts a second stage of contact between the one active area of the integrated circuit and the first level of interconnection, and consists of a single layer of metal extending from the one active area of the integrated circuit to the second stage of contact,

the second metal terminal vertically connects one active area of the integrated circuit with one plate of one of the storage capacitors, the one plate of the one storage capacitor directly contacting the upper surface of the first insulating layer, and

the third metal terminal horizontally connects two separate active areas of the integrated circuit, and consists of a single layer of metal.

20. (Currently Amended) The information processing system according to claim 19, wherein the second metal terminal has a lower surface that contacts a junction of the one active area such that the lower surface of the second metal terminal extends over a boundary of the junction of the one active area.

21. (Original) The information processing system according to claim 19, wherein the integrated circuit further comprises:

a second insulating layer above the first insulating layer; and

a cavity passing through the entire thickness of the second insulating layer and opening onto the top surface of the second metal terminal,

wherein the one plate of the one storage capacitor carpets the bottom and the inside flanks of the cavity.

22. (Original) The information processing system according to claim 21, wherein the integrated circuit further comprises:

a third insulating layer above the second insulating layer; and

a contact opening passing through the second insulating layer and the third insulating layer and opening onto the top surface of the first metal terminal.

23. (Currently Amended) The information processing system according to claim 19, wherein the first, second, and third metal terminals are made ~~principally~~ of tungsten.

24-29. (Canceled)

30. (Previously Presented) The integrated circuit according to claim 1, wherein the first insulating layer is a single layer and the only insulating layer provided between the active components and the base of the passive component.

31. (Previously Presented) The integrated circuit according to claim 1, wherein the base of the passive component directly contacts the upper surface of the first insulating layer.

32. (Previously Presented) The integrated circuit according to claim 1, further comprising:

areas of dielectric material for separating active areas that contain the active components of the integrated circuit,

wherein part of the lower surface of the metal terminal contacts one of the areas of dielectric material.

33. (Previously Presented) The integrated circuit according to claim 7, wherein the first insulating layer is a single layer and the only insulating layer provided between the transistors and a base of the passive component.

34. (Previously Presented) The integrated circuit according to claim 7, wherein the third metal terminal is a local horizontal interconnection that directly connects two separate active areas of the integrated circuit.

35. (New) The integrated circuit according to claim 1, wherein the junction of the one active component contains silicide.

36. (New) The integrated circuit according to claim 7, wherein at least some of the active areas of the integrated circuit contain silicide.

37. (New) The integrated circuit according to claim 8, wherein the second metal terminal has an upper surface that contacts the passive component, and consists of a single layer of metal extending from the junction of the one transistor to the passive component.

38. (New) The integrated circuit according to claim 37, wherein the junction of the one transistor contains silicide.